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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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26530	7590	03/04/2010	EXAMINER	
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1600 CHICAGO, IL 60604				VERDERAMO III, RALPH
2186		ART UNIT		PAPER NUMBER
03/04/2010		MAIL DATE		DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,778	XIONG, GUOPING	
	Examiner	Art Unit	
	RALPH A. VERDERAMO III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 10 November 2009.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,3,6 and 7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,3,6 and 7 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Objections

1. Claim 1 objected to because of the following informalities: Some amendment markings seem to be missing such as the added “s” in instructions and the added “for” in “...analyzing a beginning logical address for writing...” Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 now recites “receiving data write-in instructions and analyzing a beginning logical address for writing from the received data write-in **instructions...**” One interpretation of this limitation is that a plurality of write-in instructions are received and their beginning logical addresses are analyzed. Examiner cannot find support for such an interpretation in the specification. Furthermore FIG. 2 and the description of FIG. 2 seem to show a single writing operation instruction is received. Appropriate correction is required.

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4. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 3 currently seems to describe that if the other flash chip does not need to be programmed or erased it is then judged whether the first programming or erasing instructions are finished and if so returning to the processing of receiving otherwise returning to the processing of obtaining. Examiner has not found support for this flow of steps. None of the figures show a path that directly returns back to receiving or obtaining and no additional support was found in the specification.

Appropriate correction is required.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically the claim recites “detecting whether the other flash chip needs to be programmed or erased **during the first programming or erasing instructions are being processed; if need**, the method further comprises:...”

This does not seem to be proper and should be changed to increase understanding.

For example “ detecting whether the other flash chip needs to be programmed or erased **while** the first programming or erasing instructions are being processed; **if**

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programming or erasing is needed in the other flash chip, the method further comprises:..."

7. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. As explained in the new matter rejection above, claim 3 now describes that if the processing of first programming is not finished it returns to the processing of obtaining. It is not readily understood by the Examiner how this works since the obtaining processing is dependent on receiving data write-in instructions. How can one move to the obtaining processing without doing the receiving processing from which it is dependent on. This issue prevents a correct interpretation of that limitation of the claim and therefore that limitation will not be considered during examination. Appropriate correction is required.

8. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The amendment to claim 7 changed the terms "the number of written sectors" and "the number of nee-to-be-written-sectors" to "a number **for** written sectors" and "a number **for** need-to-be-written-sectors". The use of "for" here seems to be grammatically incorrect and in order to increase understanding of the claim it is requested that it be changed back to "of" in both of the cited instances.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 3, 6 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein et al. US Patent No. 5671439 (herein after referred to as Klein).

Regarding claim 1, Klein describes a data write-in method for a flash memory (It will be appreciated that other physical mass storage devices may be used...Examples include...flash memories...(column 14, line 66 – column 15, line 5)), wherein the flash memory comprises at least two flash chips (Drive A and Drive B of FIG. 2), and the method comprises: partitioning physical blocks in the flash chips to odd logical block addresses and even logical block addresses, respectively (means for alternately transferring even-numbered blocks of physical sectors between the on-board memory of the first drive and the main processing system and transferring odd-numbered blocks of physical sectors between the on-board memory of the second drive and the main processing system (column 4, lines 36 – 41)); receiving data write-in instructions and analyzing a beginning logical address for writing from the received data write-in instructions (The preferred routine preferably receives as input a starting logical sector START (column 8, lines 16 – 18). Retrieve xfer command 102 of FIG. 2. Furthermore over the course of time that this invention is operating it will retrieve a plurality of

xfer commands); obtaining the logical block address needed to be written according to the analyzed beginning logical address; determining a parity of the obtained logical block address; selecting one flash chip from the flash chips according to the determined parity of the logical block address (Starting sector on drive A? 132 of FIG. 2); directing first programming or erasing instructions to the physical blocks corresponding to the obtained logical block address in the selected flash chip (Starting sector on Drive A 132 of FIG. 2 following either YES path to Drive A Ready? 136 or NO path to Drive B Ready? 146); detecting whether the other flash chip needs to be programmed or erased during the first programming or erasing instructions are being processed (More? 142 of FIG. 2. For example first-in/first-out (FIFO) register and/or direct memory access (DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory. Then once the transfer is complete on the selected device the information from the non-selected device may be burst into or from the main memory at an extremely high rate by the FIFO and/or DMA circuitry (column 8, lines 1 – 10)); if need, the method further comprises: directing second programming or erasing instructions to the other flash chip of at least two flash chips (More? 142 of FIG. 2 following YES path to Drive B Ready? 146).

Regarding claim 3, Klein describes the data write-in method for a flash memory according to claim 1 (see above), wherein if the other flash chip does not need to be programmed or erased, the method further comprises: judging

whether the processing of the first programming or erasing instructions is finished (No path from More? 142 of FIG. 2), if yes, returning to the processing of receiving (No path from More? 142 of FIG. 2 would allow for the process to start over again and another xfer command to be retrieved in 102); otherwise returning to the processing of obtaining (As explained in the 35 USC 112 2nd rejection this limitation is considered indefinite and cannot be examined currently).

Regarding claim 6, Klein describes the data write-in method for a flash memory according to claim 1 (see above), wherein the analyzing further comprises: obtaining the number of sectors needed to be written from the data writing operation instruction (Calculate starting and total sectors for drives A & B 200 of FIG. 2).

Regarding claim 7, Klein describes the data write-in method for a flash memory according to claim 1 (see above), the analyzing further comprises judging whether the data writing operation instructions have been finished by subtracting a number for written sectors from a number for need-to-be-written sectors (338 and 340 of FIG. 5(b)).

Response to Arguments

Applicant argues with respect to claim 1 that the reference Klein has the disadvantage that two different operations cannot be performed simultaneously while the claim requires that detecting if the other flash chip needs programming or erasing happens while the first programming or erasing is being processed. Examiner explains that it is believed that Klein does teach that two operations

can be performed simultaneously. Specifically Klein describes that for example first-in/first-out (FIFO) register and/or direct memory access (DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory. Then once the transfer is complete on the selected device the information from the non-selected device may be burst into or from the main memory at an extremely high rate by the FIFO and/or DMA circuitry (column 8, lines 1 – 10).

Applicant argues with respect to claims 3, 6 and 7 that they are allowable because they depend from an allowable claim. Examiner refers to rejections and response above as to why these claims are not allowable.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-Th 7:30 - 5, every other Friday 7:30-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ralph A Verderamo III/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art
Unit 2186

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February